REMARKS

Claims 1, 3 through 5 and 7 are now pending in this application. In response to the Office Action dated March 14, 2005, independent claims 1, 5 and 7 have been amended and claims 2, 6 and 8 have been canceled. Claims 3 and 4 stand allowed. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application as now amended is respectfully solicited.

Claims 1, 5, 7 and 8 were rejected under 35 U. S. C. § 102(e) as being anticipated by U.S. patent 6,635,934 (Hidaka). The circuit of Fig. 19 has been relied upon for disclosing the elements recited in claim 1. Figs. 59 and 77 of Hidaka were relied upon with respect to the rejection of claims 5, 7 and 8. Claims 2 and 6 were rejected under 35 U. S. C. § 103(a) as being unpatentable over Hidaka in view of U.S. patent 6,256,252 (Arimoto). Arimoto has been relied upon to conclude that it would have been obvious to modify Hidaka by incorporating a switch between a power supply node and a power supply line in order to disconnect the power supply node from the power supply line for the purpose of reducing power consumption.

In response, independent claim 1 has been amended to include the recitation of now cancelled claim 2, independent claim 5 has been amended to include the recitation of now cancelled claim 6, and independent claim 7 has been amended to include the recitation of now cancelled claim 8. Favorable reconsideration in light of the following comments and withdrawal of the rejections are respectfully solicited.

With respect to the rejection of claim 2 under 35 U. S. C. § 103(a) (which now has been incorporated into claim 1), Arimoto merely discloses a single switch between power supply node VDDM and memory 80. There is no suggestion in the combined teachings of the references of a second switch circuit provided in addition to a first switch circuit as required in now amended

claim 1. In addition, there is no description related to a deep power down mode, which is expressly recited by both claims 1 and 5, in either Hidaka nor Arimoto. It is submitted, therefore, that none of the references discloses or suggests a switch for cutting off a power supply current to the second internal circuit in the deep power down mode as required by amended claim 5.

Amended claim 7 requires that the signal line is a data line for communication of storage data between the memory array and any external element. Element 150 in Figs. 59C and 64 of Hidaka is disclosed as precharge node 150 of logic circuit 155. There is no description in Hidaka that precharge node 150 corresponds to a data line. Hidaka does not disclose nor suggest that the signal line in amended claim 7 is a data line for communication of storage data.

Accordingly, it submitted that claims 1, 3 through 5 and 7 are patentably distinguishable. Withdrawal of the rejections of record and allowance of the application are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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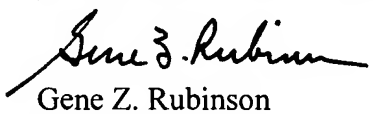

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